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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,521	07/18/2004	Yun-Ren Wang	NAUP0591USA	4520

27765 7590 06/29/2005

NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER
LINDSAY JR, WALTER LEE

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,521	WANG ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Application filed on 7/18/2004.

Currently, claims 1-20 are pending.

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grudowski (U.S. Patent No. 6,902,971 filed 7/21/2003) in view of Nakanishi et al. (U.S. Patent No. 6,884,643 filed 2/21/2003).

Grudowski shows the method as claimed in Figs. 1-10 and corresponding text as: preparing a substrate (102) (col. 3, lines 8-30); forming a gate structure (106) on said substrate, the gate structure having sidewalls and a top surface (col. 3, lines 42-54); forming an offset spacer (120) on each said sidewall of said gate structure (col. 3, line 61- col. 4, line 6); ion implanting said substrate next to said gate structure to form shallow-junction doping regions (118) (col. 4, lines 7-25); depositing a spacer layer (124); performing a stress modification implantation process to alter said spacer layer from a tensile status to a less tensile status, or into a compressive status (col. 5, lines 34-54); and dry etching said spacer layer to form spacers (col. 5, lines 55-63) (claim 1). Grudowski teaches that the substrate is a silicon substrate (col. 3, lines 31-40) (claim 2). Grudowski teaches that the gate structure is a poly gate structure (col. 3, lines 41-54) (claim 3). Grudowski teaches that a gate dielectric (104) is interposed between said gate structure and said substrate (col. 3, lines 8-30) (claim 4). Grudowski teaches that the spacer layer is made of silicon nitride (col. 4, lines 26-54) (claim 5). Grudowski teaches that the stress modification implantation process uses germanium or xenon as dopants (col. 5, lines 34-54) (claim 6). Grudowski teaches that the stress modification implantation process uses dopant species, which are electrically neutral (col. 5, lines 34-54) (claim 7). Grudowski teaches that the stress modification implantation process is carried out in an energy range of about 25 to 150 KeV (col. 5, lines 34-54) (claim 8). Grudowski teaches that the stress modification implantation process is carried out using germanium as a dopant at an implant energy of about 100 KeV and an implant dose of about 5E15 atoms/cm^2 (col. 5, lines 34-54) (claim 9). Grudowski teaches that the

shallow-junction doping regions are P type doped (col. 4, lines 7-25) (claim 10).

Grudowski shows the method as claimed in Figs. 1-10 and corresponding text as: providing a silicon substrate (102) (col. 3, lines 8-30); forming a gate structure (106) on said silicon substrate. The gate structure having sidewalls and a top surface (col. 3, lines 42-54); forming an offset spacer (120) on each said sidewall of said gate structure (col. 3, line 61- col. 4, line 6); performing a first ion implantation to implant said silicon substrate next to said gate structure so as to form first doping regions (118) acting as a source/drain extensions of said semiconductor transistor device (col. 4, lines 7-25); depositing a spacer layer (124); performing a stress modification implantation process to alter said spacer layer from a tensile status to a less tensile status, or into a compressive status (col. 5, lines 34-54); dry etching said spacer layer to form spacers (col. 5, lines 55-63); and performing a second ion implantation to implant said silicon substrate next to said spacer so as to form second doping regions (col. 6, lines 11-30) (claim 11). Grudowski teaches that the stress modification implantation process uses dopant species, which are electrically neutral (col. 5, lines 34-54) (claim 12). Grudowski teaches that the stress modification implantation process uses germanium or xenon as dopants (col. 5, lines 34-54) (claim 13). Grudowski teaches that the stress modification implantation process is carried out in an energy range of about 25 to 150 KeV (col. 5, lines 34-54) (claim 14). Grudowski teaches that the stress modification implantation process is carried out using germanium as a dopant at an implant energy of about 100 KeV and an implant dose of about 5E15 atoms/cm^2 (col. 5, lines 34-54) (claim 15). Grudowski teaches that the stress modification implantation process has a projected

range (Rp) that is smaller than said spacer layer's thickness (col. 5, lines 13-33) (claim 16). Grudowski teaches that the spacer layers thickness is about 600~700 angstroms (col. 5, lines 55-63) (claim 17). Grudowski teaches that the spacer layer is made of silicon nitride (col. 4, lines 26-54) (claim 18). Grudowski teaches that a gate dielectric (104) is interposed between said gate structure and said substrate (col. 3, lines 8-30) (claim 19). Grudowski teaches that the stress modification implantation process reduces vacancy defects of said silicon substrate (col. 1, lines 26-41) (claim 20).

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) it is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Grudowski shows the method substantially as claimed and as described in the preceding paragraphs.

Grudowski lacks anticipation only in not explicitly teaching: 1) depositing a spacer liner on said offset spacer and on said top surface of said gate structure; and depositing a spacer layer on said spacer liner (claims 1 and 11).

Nakanishi shows a method of forming a semiconductor device with an offset spacer. Nakanishi forms an offset spacer layer (4) over the gate electrode 3 (col. 6, lines 15-28). A spacer (9) is then formed over the offset spacer (4) the spacer is formed with a first TEOS layer (7) and a second layer of SiN (8) (col. 6, lines 15-28). The process aids in eliminating unexpected impurity contamination, variations in the fabrication process and to ensure high reliability (col. 1, lines 46-60).

It would be obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Grudowski by depositing a spacer liner over the offset spacer, as taught by Nakanishi, with the motivation that Nakanishi teaches that a process that aids in eliminating unexpected impurity contamination, variations in the fabrication process and to ensure high reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
June 22, 2005